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APPLICATION FOR LETTERS PATENT
(UTILITY PATENT)

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INVENTION TITLE: LOW-VOLTAGE, LOW-POWER TRANSIMPEDANCE AMPLIFIER ARCHITECTURE

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Sir:

Your applicant(s) named above hereby petition(s) for grant of a utility patent to him (them) or any assignee(s) of record, at the time of issuance, for an invention, more particularly described in the following specification and claims, with the accompanying drawings, verified by the accompanying Declaration and entitled:

Low-Voltage, Low-Power Transimpedance Amplifier Architecture

Background Of The Invention

[0001] This invention relates generally to analog circuit architecture, and, more particularly to broadband transimpedance amplifiers for converting currents to voltages.

[0002] Current trends toward the integration of electro-optic interfaces with high-speed digital integrated circuits for local and/or storage area networks and other short-haul applications require low-voltage interface circuits that can operate from available digital supplies. In order to make arrays of these interconnects efficient and a feasible alternative to electrical interconnects in server and mainframe applications, low power consumption must be also achieved. (See A. Schild, et al., "Amplifier Array for 12 Parallel 10Gb/s Optical-Fiber Links Fabricated in a SiGe Production Technology", *2002 IEEE RFIC Symposium*, pp. 89-92, 2002, incorporated herein by reference.) To avoid coding requirements for the transmitted data, a DC-coupled interface is desirable. To meet these requirements, new circuit topologies and approaches are required.

[0003] In optoelectronic communication systems, light is used to transmit data. A photodetector then converts the light signal to an electric current signal. This current signal must then be converted to a voltage signal and amplified to interface with typical digital systems. A transimpedance amplifier (TIA) is typically used for this task. (See H.-M. Rein and M. Moller "Design Considerations for Very-High-Speed Si-Bipolar IC's Operating up to 50Gb/s", *IEEE Journal of Solid-State Circuits*, vol.31, No.8, pp.1076-1090, August 1996, incorporated herein by reference.)

[0004] Traditional TIA designs, such as shown in **Figure 1**, typically use a voltage gain stage with a negative feedback resistance R_f **2** . This approach has some deficiencies for low-power, low-voltage systems at high data rates.The main problem with this approach is that, for correct operation, the input impedance of the voltage gain stage must be large. Thus, the feedback resistance R_f **2** and the voltage gain A **3** set the TIA input impedance. This means that the circuit's frequency response has a pole at the input node that is a function of the feedback

resistance (which is approximately equal to the TIA's gain for large voltage gain (A)) and the photodiode capacitance, creating a gain-bandwidth trade-off.

[0005] Equivalent input noise is another crucial performance metric for any TIA, as it sets the sensitivity limit for the receiver. As feedback resistance R_f **2** decreases, to increase the frequency of the input pole for a fixed capacitance of a photodiode **4**, the input noise increases. Therefore, a trade-off must be made in this TIA configuration between sensitivity/gain and bandwidth.

[0006] Further, the performance of such systems is limited by the performance of the voltage gain stage, which strongly effects the power consumption, the bandwidth and the required power supply voltage for the overall TIA.

[0007] Some CMOS designers have suggested using a common gate (CG) stage as a current buffer at the input, such as shown in **Figure 2**. (See S.S. Mohan, T.H. Lee, "A 2.125 Gbaud 1.6kΩ Transimpedance Preamplifier in 0.5μm CMOS", *IEEE Custom Integrated Circuits Conference 1999*, pp. 513-516, 1999.) This configuration presents an input impedance of $1/g_m$ to the photodiode **4** and allows the feedback resistance R_f **2** to be increased, as its effect is now seen by a node with a smaller capacitance.

[0008] A concern with this configuration is that a bias current path for the CG stage must still be provided and the bias path input impedance R_D **5** must be much greater than the feedback resistance R_f **2** so that the transimpedace gain is not impaired by the resulting current division. In this way, the feedback resistance is still limited by the maximum bias resistor R_b **6** value that can be used for the given power supply voltage and current requirements.

[0009] A further complication with this topology is finding a way to provide a proper bias for the CG stage over the wide range of input current levels that will be seen if the photodiode **4** is DC coupled to the TIA. This problem is amplified by the exponential response of the current to V_{be} variations in a bipolar technology, which may make it difficult to sustain a constant

collector current in a common base (CB) stage configuration with variations in DC photodiode current for a DC coupled system.

[0010] Another proposed TIA architecture uses a common-gate transistor terminated into a load and an error amplifier to adjust the common-gate operating point. That fairly complex architecture has a relatively high power consumption and larger chip area and may require the use of a higher voltage supply to accommodate the error amplifier. Furthermore, the input impedance and operating point of such a TIA remains a function of the signal applied to the input. Thus, it would be desirable to have a simplified TIA architecture that allows the TIA operating point to be independent of the input signal.

[0011] DC coupling is desirable for short-haul systems, as AC coupling may require data coding and coding results in undesired overhead (latency, power and chip area). Therefore the low frequency (LF) cut-off of the TIA must be as close to DC as possible to avoid baseline wander and ISI that would result from Fourier components of the signal falling below the LF cut-off. DC coupling can present problems in receivers due to variations in the DC input current with input signal power level affecting the bias conditions of the TIA. As such, a topology that is insensitive to these variations over a reasonable range of input power levels is desired.

Summary Of The Invention

[0012] The present invention is directed to circuits for converting an input current to an output voltage that employs a uniquely biased common-gate or common-base stage as a current buffer and a direct drive of the current buffer output into an impedance to convert the current signal to a voltage signal.

[0013] In one embodiment, the circuit comprises a low-voltage, low-power transimpedance amplifier (TIA) architecture including an NMOS field effect transistor (FET) whose source is coupled to an input node of the amplifier and whose drain is coupled to an output node of the amplifier, a diode-connected transistor serving as a floating current mirror reference, whose source is also coupled to the amplifier input node and whose gate and drain are connected to the

common gate transistor's gate. The TIA architecture further comprises a DC current source connected to the drain of the floating current reference transistor to set the common gate transistor drain current, a capacitance between the transistor gates and a DC reference voltage, a DC current path from the input node to a DC reference voltage, and a load impedance for the common gate current buffer connected between the amplifier output node and a DC reference voltage.

[0014] The current mirror reference for the current buffer floats relative to the input voltage level along with the current buffer, thus maintaining the DC current level through the common-gate buffer stage over a wide range of DC input currents.

[0015] By eliminating the voltage amplifier typically used in previous TIA architectures as described above, power consumption is significantly reduced. The circuit is also operable with much lower supply voltages than traditional architectures, at least in part due to a decrease in the number of stacked devices between the supply rails. Enhanced performance stability, with respect to changes in temperature, supply voltage and input DC power level are also attained by the present invention.

[0016] The use of transistors as current buffers allows for wider band operation than is achievable in a voltage mode circuit, allowing the inventive architecture to operate at higher speeds than traditional TIA architectures. The present invention is in no way limited to NMOS transistor usage. In alternative embodiments, the NMOS transistors are instead PMOS transistors, MESFETs, HEMTs, and/or JFETs. Additionally, the NMOS transistors may be replaced with bipolar junction transistors, such as, for example, NPN or PNP heterojunction transistors, wherein the gate- source-drain architecture is replaced with a base-emitter-collector architecture.

[0017] Other features and advantages of the invention will be apparent from the following description of the preferred embodiments thereof, and from the claims.

Brief Description of the Figures of the Drawing

[0018] For a better understanding of the present invention, reference is made to the accompanying drawing and detailed description, wherein:

[0019] **Figure 1** is a schematic of a prior art TIA employing negative feedback resistance;

[0020] **Figure 2** is a schematic of a prior art TIA employing a common gate stage as a current buffer;

[0021] **Figures 3a,3b** are schematics of MOSFET and bipolar transistor embodiments of a TIA including a common gate/base current buffer with a floating current mirror reference terminated into a transimpedance load in accordance with the present invention.

Detailed Description of Preferred Embodiments of the Invention

[0022] In a first aspect, the present invention provides transimpedance amplifier (TIA) architectures for converting an input current to a voltage. In the description below, references are made to CMOS and bipolar implementations of the TIA architectures as reflected, respectively, in **Figures 3a** and **3b**. Any disparity in the amount of text devoted to one implementation or the other arises solely from the desire for clarity, and is in no manner meant to be limiting. The concepts described apply equally well to both of these families of implementation as well as to implementations that employ devices sharing the characteristics of such transistors. The term "transistor" as used herein encompasses any device that provides a controllable output current when a voltage difference is present across its terminals, the output being current-, voltage-, optically- or mechanically-controlled. Any significant differences in alternative implementations are noted. Among alternative MOSFET embodiments, the FETs employed may comprise NMOS transistors, PMOS transistors, MESFETs, JFETs, or HEMTs. Among alternative bipolar embodiments, the bipolar transistors utilized may comprise NPN bipolar junction transistors, PNP bipolar junction transistors, NPN heterojunction bipolar transistors, and PNP heterojunction bipolar transistors.

[0023] In another aspect, the present invention provides devices incorporating such circuits, such as optical receivers that employ photodiodes to generate a current responsive to an optical input that is then converted to a voltage by the TIA architecture.

[0024] With reference to **Figure 3a**, TIA architecture **10** utilizes a uniquely biased common-gate stage **12** as a current buffer (implemented with NMOS transistor M_0 **24**), the output **13** of which directly drives a load impedance Z_T **14** coupling the drain of transistor M_0 **24** to a DC reference or supply voltage V_{DD} **36**. Architecture **10** converts the alternating component I_{ac} of the input current signal I_{in} **15**present at input node **34** into an output voltage signal V_{out} **17**. The unique biasing scheme makes use of a current mirror reference **16** for the current buffer, implemented with NMOS transistor M_1 **26** that is fed at its drain by a DC current source **18**. Current mirror reference **16** floats relative to the input voltage level (at input node **34**) along with the current buffer as the voltage drop across a DC current path created by resistance R_B **21** changes with variations in the DC input current I_{DC} of input current signal I_{in} **15**. This maintains the DC current level through the current buffer stage **12** over a wide range of DC input currents I_{DC}, maintaining its DC operating point.

[0025] A number of advantages are attained through the use of this unique biasing scheme and direct drive into a transimpedance resistor (load impedance Z_T **14**), rather than using a voltage gain stage with feedback as is traditionally done. By eliminating voltage amplifiers typically used in TIA architectures, power consumption is significantly reduced and the maximum circuit gain can be achieved for a given bandwidth. The TIA architecture **10** operates from much lower supply voltages than traditional architectures, due to a decrease in the number of stacked devices between the supply rails. Excellent performance stability, with respect to changes in temperature, supply voltage and input DC power level, is achieved due to the insensitivity of the circuit transfer function to these variables. The use of the transistors as current buffers allows for wider band operation than could be achieved in a voltage mode circuit, which allows this architecture to operate at higher speeds than other architectures, when implemented in the same technology. Through the maintenance of the DC operating point as the

input current level varies the circuit's broadband input impedance is maintained and the DC voltage at the output is also stabilized as the DC current through the load impedance is held constant and hence so is the voltage drop across it.

[0026] When the TIA architecture **10** is used with a photodetector **28** as an optoelectronic receiver, the photodetector capacitance sees an input impedance of $1/g_{m0}$, as M_0 **24** is a common gate buffer stage **12**, due to the (preferably high) capacitance **22** at the gates of NMOS transistors M_0 **24** and M_1 **26** (or the bases of bipolar transistors Q_0 **38** and Q_1 **36** in the bipolar embodiment of **Figure 3b)**. The current I through the common gate stage **12**, which sets $1/g_{m0}$, is held constant by the floating current mirror reference **16**. By coupling the sources **30,32** of the transistors M_0 **24** and M_1 **26** and input node **34** together, the drain current in common-gate stage **12** is held constant regardless of variations in the input DC current I_{DC} level (*e.g.*, from the anode of the photodetector **28**), which will change the current flowing through the DC current path **20** (and shunted through R_B **21**) and shift the DC voltage at input node **34**, without affecting the drain current. In this way the TIA architecture's input impedance is held constant, as it is determined by the buffer current and physical characteristics of the transistors. The output DC voltage V_{out} **17** is also kept constant despite variations in the photodiode DC input current I_{DC}, as the DC current through load impedance Z_T **14** is held constant and hence so is the DC voltage drop across it. As such, the overall performance of the TIA architecture **10** is relatively insensitive to variations in the DC current I_{DC} from the photodetector **28**.

[0027] By selecting a ratio of *n* between the sizes of current mirror transistor M_1 **26** and the common-gate transistor M_0 **24**, the excess bias current from the current mirror transistor M_1 **26** can be minimized and its input impedance can be set high enough to avoid degrading the common-gate transistor M_0 **24** signal current transfer (*i.e.*, the input impedance of the current mirror transistor M_1 **26** will be approximately *n* times the input impedance of the common-gate transistor M_0 **24** due to their drain current ratio.)

[0028] In alternative embodiments, the NMOS FETs shown in **Figure 3a** may instead comprise PMOS FETs if the polarity of DC reference (supply) voltages V_{DD} **36** are reversed

(*i.e.*, if a negative voltage V_{DD} is used.) In yet other embodiments, the FETs comprise MESFETs, JFETs, and HEMTs. Similarly, the NPN bipolar transistors **36,38** shown in **Figure 3b** may alternatively comprise other types of transistors, such as PNP bipolar junction transistors, heterojunction bipolar transistors, NPN heterojunction bipolar transistors, and/or PNP heterojunction bipolar transistors. As noted above, other devices with properties similar to these transistors may also be used in place of the NMOS FETs depicted in the preferred embodiment, as would be apparent to persons skilled in the art.

[0029] R_B **21** should be set as large as possible, to avoid excess noise, while still providing sufficient DC reverse bias for the photodetector **28** and keeping M_1 **26** (or Q_1 **36**) in the forward active region over all photodetector DC operating currents I_{DC}. It should be noted that gain is not a function of drain/collector current in this configuration. Achieving a reasonable input impedance for the TIA (setting an appropriate input pole) requires less than 1mA of collector current in a bipolar implementation for 12.5Gb/s operation and similar current levels can be used in a CMOS implementation. At such an operating point, g_{m0}=40mS at room temperature for a bipolar junction transistor. In this example, the entire TIA architecture **10** can be operated using only ~1mA of current, which is much less than conventional TIAs. This decreases power consumption and also the voltage drop across the resistors in the circuit, allowing them to be made larger to decrease noise or allowing the supply voltage to be scaled.

[0030] Terminating directly into the load impedance Z_T, rather than the feedback resistor and the bias load, also allows a larger impedance to be achieved for a given V_{DD} than with conventional TIAs.

[0031] It should be noted that in a preferred embodiment resistors are used for R_B and Z_T rather than MOSFETs to bias the circuit or provide active loads due to the their noise advantage. If we compare the noise of a resistor to that of a MOSFET, it can be found that the resistor provides lower noise (for a given V_{ds} or voltage drop across the resistor) unless:

$$Vgs - Vt > 2\Gamma Vds, \qquad \textbf{Eqn. 1}$$

where Γ is the excess noise factor (2/3 in long-channel devices and larger in short channel devices). But for a MOSFET in saturation we require:

$$Vgs - Vt < Vds . \qquad \textbf{Eqn. 2}$$

[0032] Thus, a MOSFET in saturation always generates more noise as a load than an equivalent resistor. Therefore, resistors are used for R_B and Z_T. Some inductance may be used in series with the load in order to provide bandwidth extension.

[0033] For a more detailed discussion of the theoretical principles and simulation results of the TIA architecture **10** , including a discussion of the frequency response and noise determination and minimization analysis of the circuit, see Guckenberger and Kornegay, "Novel Low-Voltage, Low-Power Gb/s Transimpedance Amplifier Architecture", *VLSI Circuits and Systems, 2003, Proc. Of SPIE*, Vol. 5117, pp. 274-285, incorporated herein by reference in its entirety. Summarizing part of the discussions therein, the broadband transimpedance gain of the circuit can be shown to be approximately equal to the value of a resistor R_T coupling the drain/collector of M_0/Q_0 to the DC reference voltage **36**, and that only the temperature coefficient of R_T affects the broadband gain significantly. By using a polysilicon resistor with a low temperature coefficient of resistivity, a very stable thermal response can be achieved.

[0034] This architecture offers very low power consumption, while providing the ability to operate from lower power supply voltages than traditional TIAs. Simulation results for 0.25μm CMOS and 47GHz f_T SiGe BiCMOS TIA implementations demonstrate that low-power, low-voltage operation can be achieved using this architecture at data rates up to 12.5Gb/s, which is believed to be the highest data rate reported for a 0.25μm CMOS TIA. The 1.8V supply used for the SiGe BiCMOS implementation is believed to be the lowest supply voltage reported for a bipolar implementation.

[0035] Although the invention has been described with respect to various embodiments, it should be realized this invention is also capable of a wide variety of further and other embodiments within the spirit of the invention.

[0036] What is claimed is: